What is claimed is:

1. A composition of matter, comprising:

a substrate having a surface; and

a multilayer structure formed on the surface of the substrate, the multilayer structure comprising multiple superposed layer pairs, each layer pair consisting of a first layer of silicon and a second layer of nickel and having a layer-pair thickness of 3.0 nm or less.

2. The composition of claim 1, wherein the substrate is selected from the group consisting of semiconductor materials, metals, glass materials, crystalline materials, and ceramic materials.

3. The composition of claim 2, wherein the surface of the substrate is a surface of a silicon layer applied to the substrate.

4. The composition of claim 1, wherein the substrate is silicon.

5. The composition of claim 1, exhibiting an electrical conductivity, from the multilayer structure to the substrate, of less than 13 $\mu\Omega$·cm.

6. The composition of claim 1, wherein the multilayer structure comprises two to ten layer pairs.

7. The composition of claim 1, wherein the multilayer structure comprises more than 50 mole-percent of nickel.

8. The composition of claim 1, wherein the multilayer structure comprises substantially equal mole percentages of silicon and nickel.

9. The composition of claim 1, further comprising a capping layer superposed on the multilayer structure.

10. The composition of claim 7 wherein the capping layer is a layer of nickel.

11 The composition of claim 1, wherein the multilayer structure is an amorphous phase of silicon and nickel.

12 The composition of claim 11 wherein the multilayer structure is amorphous NiSi.

13 The composition of claim 12 further comprising a metal capping layer superposed on the multilayer structure.

14 The composition of claim 13 wherein the metal is nickel.

15 The composition of claim 1, wherein the multilayer structure is crystalline SiNi.

16. The composition of claim 15, further comprising a nickel capping layer.

17. A method for making a compound of nickel and silicon, comprising:

on a surface of a substrate, forming multiple layer pairs in a superposed manner, each layer pair comprising a respective layer of nickel and a respective layer of silicon each being 3 nm or less in thickness, wherein the layers of nickel and silicon in the multiple layer pairs are formed in alternating order, thereby forming a multilayer structure, wherein the layers of nickel and silicon in the multilayer structure are formed at respective thicknesses corresponding to desired mole fractions of nickel and silicon in the multilayer structure;

annealing the multilayer structure at an annealing temperature of 200 °C or less to form an amorphous alloy of nickel and silicon in the multilayer structure, the alloy having the desired mole fractions of nickel and silicon; and

allowing the amorphous alloy to nucleate and form a corresponding crystalline alloy.

18. The method of claim 17, wherein the crystalline alloy has the desired mole fractions of nickel and silicon

19. The method of claim 17, wherein the step of allowing the amorphous alloy to nucleate is performed by annealing the amorphous alloy at an annealing temperature of 350 °C or less.

20. The method of claim 19, wherein the step of annealing the amorphous alloy comprises, at onset of annealing, ramping up to the annealing temperature of 350 °C or less.

21. The method of claim 17, wherein the step of forming the multiple layer pairs is performed on a substrate selected from the group consisting of semiconductor materials, glass materials, ceramic materials, crystalline materials, and metal materials.

22. The method of claim 17, wherein the step of forming the multiple layer pairs is performed on a substrate having a silicon surface.

23. The method of claim 22, further comprising the step of cleaning the silicon surface before forming the multilayer structure on the silicon surface.

24. The method of claim 22, wherein the substrate is silicon.

25. The method of claim 17, wherein the step of forming the multiple layer pairs comprises forming two to ten layer pairs.

26. The method of claim 17, wherein the layers of silicon and nickel are formed at respective thicknesses sufficient to form the multilayer structure having substantial equal mole percentages of nickel and silicon.

27. The method of claim 17, wherein the layers of silicon and nickel are formed at respective thicknesses sufficient to form the multilayer structure having more than 50 mole-percent of nickel.

28. The method of claim 17, further comprising the step of forming a capping layer superposedly on the multilayer structure.

29. The method of claim 28, wherein the capping layer is a layer of nickel.

30. The method of claim 17, wherein each of the nickel layers and each of the silicon layers is formed by electron beam evaporation.

31. A compound of nickel and silicon formed by the method recited in claim 17.

32. The compound of claim 31, wherein the compound is a crystalline alloy of silicon and nickel.

33. In a microelectronic-device fabrication method, a method for providing a silicon-containing active-circuit element with a low-resistivity contact, the method comprising:

on a region of the surface of the active-circuit element, forming multiple layer pairs in a superposed manner, each layer pair comprising a respective layer of nickel and a respective layer of silicon each being 3 nm or less in thickness, wherein the layers of nickel and silicon in the multiple layer pairs are formed in alternating order, thereby forming a multilayer structure, wherein the layers of nickel and

silicon in the multilayer structure are formed at respective thicknesses corresponding to desired mole fractions of nickel and silicon in the multilayer structure;

annealing the multilayer structure at an annealing temperature of 200 °C or less to form an amorphous alloy of nickel and silicon in the multilayer structure, the alloy having the desired mole fractions of nickel and silicon; and

allowing the amorphous alloy to nucleate and form a corresponding crystalline alloy.

34. The method of claim 33, wherein the crystalline alloy has the desired mole fractions of nickel and silicon.

35. The method of claim 33, further comprising the step, after forming the crystalline alloy, of connecting a metal conductor to the crystalline alloy so as to establish a low-resistivity contact between the active-circuit element and the metal conductor.

36. The method of claim 33, further comprising the step of forming a capping layer on the multilayer structure before annealing the multilayer structure.

37. The method of claim 36, wherein the capping layer is a layer of nickel.

38. The method of claim 36, further comprising the step, after forming the crystalline alloy, of connecting a metal conductor to the crystalline alloy so as to establish a low-resistivity contact between the active-circuit element and the metal conductor.

39. The method of claim 33, wherein the step of allowing the amorphous alloy to nucleate is performed by annealing the amorphous alloy at an annealing temperature of 350 °C or less.

40. The method of claim 39, wherein the step of annealing the amorphous alloy comprises, at onset of annealing, ramping up to the annealing temperature of 350 °C or less.

41. The method of claim 33, further comprising the step of cleaning the surface of the active-circuit element before forming the multilayer structure on the silicon surface.

42. The method of claim 33, wherein the step of forming the multiple layer pairs comprises forming two to ten layer pairs.

43. The method of claim 33, wherein the layers of silicon and nickel are formed at respective thicknesses sufficient to form the multilayer structure having substantial equal mole percentages of nickel and silicon.

44. The method of claim 33, wherein the layers of silicon and nickel are formed at respective thicknesses sufficient to form the multilayer structure having more than 50 mole-percent of nickel.

45. The method of claim 33, wherein each of the nickel layers and each of the silicon layers is formed by electron beam evaporation.

46. A microelectronic device, comprising low-resistivity contacts formed as recited in claim 33.